UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/897,574	07/02/2001	Kenichi Kawaguchi	10873.744US01	1221

53148	7590	09/19/2005	

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EXAMINER
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ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _14 January 2005_.

2a)☐ This action is **FINAL**.　　2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-14_ is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-14_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _07 February 2001_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All　b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1.   Receipt is acknowledged of the request filed on 13th of July 2005 for a request

for continued examination (RCE) under 37 CFR 1.114 based on the application No.

09/897574, which the request is acceptable and an RCE has been established.

Currently, claims 1-14 are pending in this application.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3.   Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by West

(US Patent 6,195,730)

As per claims 1, 6 West discloses a data transfer apparatus comprising:

- An associative memory(fig.1, 46 ie IOP local memory) connected between

   a system bus(fig.1, 28 ie system bus) and a local bus(fig.1, 36 ie IOP

   expansion bus); and (col.4, lines 38-60)

- A controller(fig.1, 44 ie IOP microprocessor) for controlling data

   input/output of the associative memory; (col.3, lines 1-16)

- Wherein the controller fetches an address and data that are transferred between devices (fig.1, 26, ie IOP) that are connected only on the system bus so as to duplicate and store them in the associative memory, (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

- When a device (fig.1, 22 ie storage device) on local bus generates a read cycle to read data from a read address associated with one of the devices on the system bus and the read address is contained in the address stored in the associative memory, the controller reads out corresponding data from the associative memory so as to transfer it to the local bus. (col.3, lines 1-46 ie any storage devices is required for the data transfer, the request is mapped in the cache memory to the storage devices capable of servicing the request and transferring via IOP expansion bus(local bus)), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

As per claims 2, 7, West discloses wherein if it is detected that a write cycle of writing a data from one device to another device is generated on the system bus, the controller fetches the address and the data that are transferred between the devices so as to duplicate and store them in the associative memory. (col.3, lines 1-45)

As per claims 3,8, West discloses wherein the controller monitors a data output enable signal line of at lest one device controller on the system bus and, when the data output enable signal line is asserted, fetches the address and the data

that are transferred on the system bus so as to duplicate and store them in the associative memory. (col.3, lines 1-45)

As per claims 4,9, West discloses wherein the controller monitors a data output strobe signal line of at least one device controller on the system bus and, when the data output strobe signal line is asserted, fetches the address and the data that are transferred on the system bus so as to duplicate and store them in the associative memory. (col. 3, lines 1-45)

As per claims 5, 10, West discloses wherein when the address from which the data is transferred indicated by the data transfer request accepted from the local bus is not contained in the address stored in the associative memory, the controller stores a data effective information indicating the address in which a transfer operation has not been completed in response to the data transfer request in a second associative memory, fetches the address and the data that are transferred between the devices on the system bus and, if the fetched address is the address indicated by the data effective information, transfers it to the local bus as data corresponding to the data transfer request. (col.7, line 66-col.9, line 34 ie controller maps the data transfer request to cache device (correlates mapping table) and determine whether or not the requested data is currently contained within cache memory)

As per claim 11, West discloses a data transfer apparatus comprising:

- An associative memory (fig.1, 46 ie IOP local memory) connected

  between a system bus(fig.1, 28 ie system bus) and a local bus fig.1, 36 ie

  IOP expansion bus); and (col.4, lines 38-60)

- A controller for controlling data input/output of the associative memory;

- A controller(fig.1, 44 ie IOP microprocessor) for controlling data

  input/output of the associative memory; (col.3, lines 1-16)

- Wherein the controller fetches an address and data that are transferred

  between devices (fig.1, 26, ie IOP) that are connected only on the system

  bus so as to duplicate and store them in the associative memory, (col.3,

  lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

- Fetches an address and a data that are transferred between devices on

  the local bus so as to duplicate and store them in the associative memory,

  (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory

  62)

- When a device(fig.1, 22 storage device) on the local generates a read

  cycle to read data from a read address associated with one of the devices

  on the system bus and the read address is contained in the address

  stored in the associative memory, the controller reads out a corresponding

  data from the associative memory so as to transfer it to the local, accepts

  a data transfer request from the system bus and, when an address from

  which the data is transferred indicated by the data transfer request it

contained in the address stored in the associative memory, reads out

corresponding data from the associative memory so as to transfer it to the

system bus. (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie

cache memory 62)

As per claim 12, West discloses a data transfer method for controlling data

input/output between a system bus and a local bus the method comprising:

- A buffering operation of fetching an address and data that are

  transferred between devices on the system bus so as to duplicate and

  store them; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line

  22, ie cache memory 62)

- An operation of accepting a data transfer request from the local bus

  when a device on the local bus generates a read cycle to read data

  from a read address associated with one of the devices on the system

  bus and the read address is contained in the address stored in the

  buffering operation; and (col.3, lines 35-45), (also see col.5, line 11-

  col.6, line 22, ie cache memory 62)

- Reading out corresponding data so as to transfer it to the local bus.

  (col.3, lines 1-46 ie any storage devices is required for the data

  transfer, the request is mapped in the cache memory to the storage

  devices capable of servicing the request and transferring via IOP

expansion bus(local bus)), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

As per claim 13, West discloses a data transfer method for controlling data input/output between a system bus and a local bus, the method comprising:

- A buffering operation of fetching an address and data that are transferred between devices that are connected only on the local bus so as to duplicate and store them; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

- An operation of accepting a data transfer request from the system bus and, when a device on the system bus generates a read cycle to read data from a read address associated with one of the devices on the local bus and the read address is contained in the address stored in the buffering operation; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

- Reading out corresponding data so as to transfer it to the system bus. (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory 62)

As per claim 14, West discloses a data transfer method for controlling data input/output between a system bus and a local bus, comprising:

- A first buffering operation of fetching an address and data that are
  transferred between devices (fig.1, 26 ie IOP) that are connected only on
  the system bus(fig.1, 28 ie system bus) so as to duplicate and store them;
  (col.3, lines 35-45), (also see col.5, line 11-col.6, line 22, ie cache memory
  62)

- A second buffering operation of fetching an address and data that are
  transferred between devices (fig.1, 22 ie storage devices) which are
  connected only on the local bus(fig.1, 36 ie IOP expansion bus) so as to
  duplicate and store them; (col.3, lines 35-45), (also see col.5, line 11-col.6,
  line 22, ie cache memory 62)

- A first data transfer operation of accepting a data transfer request from the
  local bus and, when a device on the local bus generates a read cycle to
  read data from a read address associated with one of the devices on the
  system bus and the read address is contained in the address stored in the
  first buffering operation, reading out corresponding data so as to transfer it
  to the local bus; and (col.3, lines 35-45), (also see col.5, line 11-col.6, line
  22, ie cache memory 62)

- A second data transfer operation of accepting a data transfer request from
  the system bus when a device on the system bus generates a read cycle
  to read data from a read address associated with one of the devices on
  the local bus and the read address is contained in the address stored in
  the second buffering operation, reading out corresponding data so as to

transfer it to the system bus. (col.3, lines 35-45), (also see col.5, line 11-

col.6, line 22, ie cache memory 62)

Response to Amendment

4.   Applicant's amendment filed on 7/7/05 have been fully considered but are moot

in view of the new ground(s) of rejection.

Conclusion

5.   *Any inquiry concerning this communication or earlier communications from the examiner should*

be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to

[kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to

reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be

reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].

The fax phone numbers for the organization where this application or proceeding is assigned are

(571)273-8300 for regular communications and After Final communications. Any inquiry of a general

nature or relating to the status of this application or proceeding should be directed to the receptionist

whose telephone number is (571)272-2100.

Kim Huynh

September 14, 2005